"Education for Knowledge, Science and Culture" -
Shikshanmaharshi Dr. Bapuji Salunkhe

Shri Swami Vivekanand Shikshan Sanstha's

VIVEKANAND COLLEGE (AUTONOMOUS), KOLHAPUR.

B. Sc. Part – I CBCS Syllabus with effect from June, 2018
ELECTRONICS-DSC -1005 A
Semester: I Electronics-Paper- I
NETWORK ANALYSIS AND ANALOG ELECTRONICS

Theory: 60 Hours (75 lectures of 48 minutes) - Credits -4

Section-I

UNIT – 1

Circuit Analysis: **(14 Lectures.)**

Concept of Voltage and Current Sources. Kirchhoff's Current Law, Kirchhoff's Voltage Law. Mesh Analysis. Node Analysis. Principle of Duality. Superposition Theorem. Thevenin's Theorem. Norton's Theorem. Reciprocity Theorem. Maximum Power Transfer Theorem. Millman's Theorem.

UNIT – 2 Two Port Networks: **(5 Lectures.)**

Concept of two port network .Z, Y and h parameters and their equivalent circuits and their conversion.Star and Delta networks, Star-Delta Conversion.

UNIT – 3 PN Junction Diode: **(8Lectures.)**

Construction of PN junction, Formation of Depletion Layer, Barrier potential, Diode Equation and I-V characteristics, static and dynamic resistance, dc load line analysis, Quiescent (Q) point.Zener diode, Reverse saturation current, Zener and avalanche breakdown.Schottky diode and it's characteristics.

UNIT – 4 D.C. Power Supply : **(10Lectures.)**

Block diagram of D.C.regulated power supply, Rectifiers: Half wave , Full wave rectifiers (center tapped andbridge), circuit diagrams, working and waveforms, ripple factor and efficiency. Filter-Shunt capacitorfilter, its role in power supply, output waveform, and working. Regulation- Line and load regulation, Zener diode as voltage regulator,
Three pin IC regulators: Block diagram, Fixed and Variable voltage IC regulator.
Concept of SMPS

Section-II

UNIT- 1

Bipolar Junction Transistor: **(10Lectures.)**

Introduction, Structure of BJT, Working of transistor, Transistor configurations: CB, CE and CC configurations, characteristics of transistor in CE and CBconfigurations, Regions of operation (active, cut off and saturation), Current gains α andβ. Relations between α and β. dc load line and Q point (Operating point).

UNIT – 2

Unipolar Devices: **(6Lectures.)**

JFET.Construction, working and I-V characteristics (output and transfer), Pinchoff voltage.UJT, basic construction, working, equivalent circuit and I-V characteristics.

UNIT -3

Amplifiers: **(16Lectures.)**

Transistor biasing and Stabilization circuits- Fixed Bias and Voltage
Divider Bias. Thermal runaway, stability and stability factor S. Transistor as a two port network, h-parameter equivalent circuit. Small signal analysis of single stage CE amplifier. Input and Output impedance, Current and Voltage gains. Class A, B, AB and C Amplifiers(Comparative Study)

Cascaded Amplifiers: Two stage RC Coupled Amplifier and its Frequency Response.

UNIT- 4

FeedbackAmplifier and Oscillators: **(6 Lectures.)**

Concept of feedback, negative and positive feedback, advantages of negative feedback (Qualitative only).

Sinusoidal Oscillators: Barkhausen criterion for sustained oscillations. Phase shift, Hartley and Colpitt's oscillator. Determination of Frequency and Condition of oscillation.

Reference Books:

1. A text book of Applied Electronics, R.S.Sedha (S.Chand& Company)
2. Basic Electronics and Linear circuits, N.N.Bharagava, D.C.Kulshreshtha and S.C.Gupta (TMH)
3. Electronic Devices and Circuits, J.Millman & C.C. Halkias (TMH)
4. Electronic Devices and Circuits, Allen Mottershead (PHI)
5. Basic solid state Electronics, B.L.Theraja (S.Chand & Company)
6. Basic Electronics, Bernard Grob,(McGraw-Hill)

ELECTRONICS-DSC -1005 B
Semester: II Electronics-Paper- II
LINEAR AND DIGITAL INTEGRATED CIRCUITS
Theory: 60 Hours(75 lectures of 48 minutes -Credits -4

Section-I

UNIT – 1 Operational Amplifier: (**17 Lectures**)
Concept of differential amplifier, Characteristics of an Ideal and Practical Operational Amplifier, study of IC 741, Open and closed loop configuration, Frequency Response .CMRR, Slew Rate and concept of Virtual Ground. Applications of Op-Amps: (1) Inverting and non-inverting amplifiers, (2) Summing and Difference Amplifier, (3) Differentiator, (4) Integrator, (5) Wein bridge oscillator,(6) Comparator and Zero-crossing detector, and (7) Active low pass and high pass. Study of LM 358,TLC 271(Salient feature and pin configuration)

UNIT – 2 Clock and Timer (IC 555): (**6 Lectures**)
Introduction, Block diagram of IC 555, Monostable, Bistable and Astable multivibrator circuits.

UNIT – 3 Combinational circuits: (**8 Lectures**)
Multiplexers: - 2 to 1, 4 to 1 and 8 to 1.Demultiplexers: - 1 to 2,1 to 4, 1 to 8. Encoder: concept of encoder, Decimal to BCD Encoder. Basic Binary decoders: 2 to 4 line, 3 to 8 line and 4 to 16 line,BCD to decimal decoder, BCD to seven-segment decoder driver, IC 7447.

UNIT – 4 D-A and A-D Conversion: (**6 Lectures**)
4 bit binary weighted and R-2R D-A converters, circuit and working. Accuracy and Resolution. A-D conversion characteristics, successive approximation ADC, Single slope and dual slope ADC

Reference Books:

1. OP-Amps and Linear Integrated Circuit, R. A. Gayakwad, 4th edition, 2000, Prentice Hall
2. Digital Principles and Applications, A.P. Malvino, D.P.Leach and Saha, 7th Ed., 2011,
    a. Tata McGraw
3. Digital Fundamentals, Thomas L. Flyod, Pearson Education Asia (1994)

Section-II

Unit – 1 Number System and Codes: (**8 Lectures**)
Decimal, Binary, Octal and Hexadecimal number systems, base conversions.Representation of signed and unsigned numbers, BCD code. ASCII code, Binary,octal and hexadecimal arithmetic; addition, subtraction by 2's complement method,multiplication.

Unit – 2 Logic Gates, Boolean algebra and logic analysis: (**12 Lectures**)
Truth Tables of OR, AND, NOT, NOR, NAND,XOR, XNOR, Universal Gates, Basic postulates and fundamental theorems of Booleanalgebra.Standard representation of logic functions(SOP and POS), Minimization Techniques (Karnaugh map minimization up to 4variables for SOP).
Arithmetic Circuits: Binary Addition. Half and Full Adder. Half and Full Subtractor, 4-bit binary Adder/Subtractor.

Unit – 3 Sequential Circuits: (**9 Lectures**)
SR, D, and JK Flip-Flops. Clocked (Level and Edge Triggered)Flip-Flops. Preset and Clear operations. Race-around conditions in JK Flip-Flop.Master-slave JK Flip-Flop, T-Flip-flop

Unit – 4 Shift registers and Counters: (**9 Lectures**)
Serial-in-Serial-out, Serial-in-Parallel-out, Parallel-in-Serial-out andParallel-in-Parallel-out Shift Registers (only up to 4 bits).
Counters (4 bits**):** Ring Counter. Asynchronous counters, Decade Counter.Synchronous Counter.

Reference Books:

1. Digital Fundamentals Floyd.
2. Digital Principles and Applications A.P.Malvino & D.P.Leach (TMH).
3. Modern digital Electronics (2nd Edn.) R.P.Jain.

ELECTRONINCS LAB(I) : DSC -1005A(pr)

Semester: I
NETWORK ANALYSIS AND ANALOG ELECTRONICS
60 Hours(75 lectures of 48 minutes) - Credits -2

AT LEAST 08 EXPERIMENTS FROM THE FOLLOWING

1. To familiarize with basic electronic components (R, C, L, diodes, transistors), Digital Multimeter, Function Generator and Oscilloscope.
2. Measurement of Amplitude, Frequency & Phase difference using Oscilloscope.
3. Verification of (a) Thevenin's theorem and (b) Norton's theorem.
4. Verification of Superposition Theorem .
5. Verification of the Maximum Power Transfer Theorem.
6. Study of the I-V Characteristics of (a) p-n junction Diode, and (b) Zener diode.
7. Study of (a) Half wave rectifier and (b) Full wave rectifier (FWR).
8. Study the effect of (a) C- filter and (b) Zener regulator on the output of FWR.
9. Study of the I-V Characteristics of UJT and design relaxation oscillator..
10. Study of the output and transfer I-V characteristics of common source JFET.
11. Study of Fixed Bias and Voltage divider bias configuration for CE transistor.
12. Design of a Single Stage CE amplifier of given gain.
13. Study of the RC Phase Shift Oscillator.
14. Study the Colpitt`s oscillator/Hartley oscillator.

SPICE/MULTISIM simulations for electronic circuits and devices

AT LEAST 02 EXPERIMENTS FROM THE FOLLOWING

1. To verify the Thevenin and Norton Theorems.
2. Design and analyze the series and parallel LCR circuits
3. Design the inverting and non-inverting amplifier using an Op-Amp of given gain
4. Design and Verification of op-amp as integrator and differentiator
5. Design the 1st order active low pass and high pass filters of given cutoff frequency
6. Design a Wein`s Bridge oscillator of given frequency.
7. Design clocked SR and JK Flip-Flop`s using NAND Gates
8. Design 4-bit asynchronous counter using Flip-Flop ICs.
9. Design the CE amplifier of a given gain and its frequency response.

Reference Books

1. Digital Principles and Applications, A.P. Malvino, D.P.Leach and Saha, 7th Ed., 2011,Tata McGraw
2. OP-Amps and Linear Integrated Circuit, R. A. Gayakwad, 4th edn., 2000, Prentice Hall
3. Lab manual.

ELECTRONICS LAB(II) : DSC -1005B (pr)
Semester: II
LINEAR AND DIGITAL INTEGRATED CIRCUITS
62 Hours(75 lectures of 48 minutes)- Credits-2

At least 05 experiments each from section A, B

Section-A: Op-Amp. Circuits (Hardware)

1. To design an inverting amplifier using Op-amp (741/351)for dc voltage of given gain
2. (a) To design inverting amplifier using Op-amp (741/351) & study its frequency response
(b) To design non-inverting amplifier using Op-amp (741/351) & study frequency response
3. (a) To add two dc voltages using Op-amp in inverting and non-inverting mode
(b) To study the zero-crossing detector and comparator.
4. To design a precision Differential amplifier of given I/O specification using Op-amp.
5. To investigate the use of an op-amp as an Integrator.
6. To investigate the use of an op-amp as a Differentiator.
7. To design a Wien bridge oscillator for given frequency using an op-amp.
8. Design a digital to analog converter (R-2R DAC) of given specifications.

Section-B: Digital circuits (Hardware)

1. (a) To design a combinational logic system for a specified Truth Table.
(b) To convert Boolean expression into logic circuit & design it using logic gate ICs.
(c) To minimize a given logic circuit.
2. Half Adder and Full Adder.
3. Half Subtractor and Full Subtractor.
4. 4 bit binary adder and adder-subtractor using Full adder IC.
5. To design a seven segment decoder.
6. To design an Astable Multivibrator of given specification using IC 555 Timer.
7. To design a Monostable Multivibrator of given specification using IC 555 Timer.
8. To build Flip-Flop (RS, Clocked RS, D-type and JK) circuits using NAND gates.
9. To build JK Master-slave flip-flop using Flip-Flop ICs
10. To build a Counter using D-type/JK Flip-Flop ICs and study timing diagram.
11. To make a Shift Register (serial-in and serial-out) using IC 7495.

Reference Books

1. Digital Principles and Applications, A.P. Malvino, D.P.Leach and Saha, 7th Ed., 2011,Tata McGraw
2. OP-Amps and Linear Integrated Circuit, R. A. Gayakwad, 4th edn., 2000, Prentice Hall
3. Lab manual.

Nature of Question Paper

***Instructions*:** *1) All the questions are **compulsory**.*

*2) Answers to the two sections should be written in **same** answer book.*

*3) Figures to the right indicate **full** marks.*

*4) Draw neat labeled diagrams **wherever** necessary.*

5) Use of log table/calculator is allowed.

Time : 3 hours **Total Marks: 80**

SECTION-I

Q.1. Choose correct alternative. **8**

i)

A) B) C) D)

ii)

A) B) C) D)

iii)

A) B) C) D)

iv)

A) B) C) D)

v)

A) B) C) D)

vi)

A) B) C) D)

vii)

A) B) C) D)

viii)

A) B) C) D)

Q.2. Attempt any two. **16**

A)

B)

C)

Q.3. Attempt any four. **16**

a)

b)

c)

d)

e)

SECTION-II

Q4. Choose correct alternative. **8**

i)

A) B) C) D)

ii)

A) B) C) D)

iii)

A) B) C) D)

iv)

A) B) C) D)

v)

A) B) C) D)

vi)

A) B) C) D)

vii)

A) B) C) D)

viii)

A) B) C) D)

Q.5. Attempt any two. **16**

A)

B)

C)

Q.6. Attempt any four. **16**

a)

b)

c)

d)

e)

f)

SCHEME OF MARKING (THEROY)

Sem.	DSC	Marks	Evaluation	Sections	Answer Books	Standard of passing
I	DSC1005 A	80	Semester wise	Two sections each of 40 marks	As per Instruction	35% (28 marks)
II	DSC1005 B	80	Semester wise	Two sections each of 40 marks	As per Instruction	35% (28marks)

SCHEME OF MARKING (CIE) Continuous Internal Evaluation

Sem.	DSC	Marks	Evaluation	Sections	Answer Books	Standard of passing
I	DSC1005 A	20	Concurrent	-	As per Instruction	35% (7 marks)
II	DSC1005 B	20	Concurrent	-	As per Instruction	35% (7 marks)

SCHEME OF MARKING (PRACTICAL)

Sem.	DSC	Marks	Evaluation	Sections	Standard of passing
I AND II	DSC1005 A(pr)	50	Annual	As per Instruction	35% (18 marks)
	DSC1005 B(pr)				

***A separate passing is mandatory**